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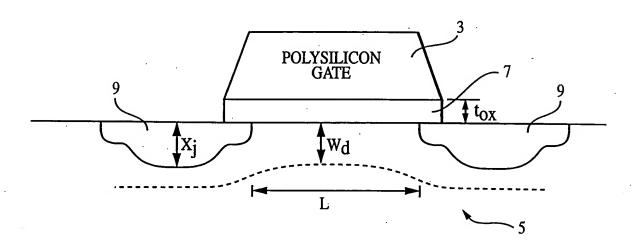
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App No.: Not Yet Assigned Inventor: Leonard Forbes et al. Docket No.: M4065.0381/P381-A

Title: TECHNIQUE TO MITIGATE SHORT CHANNEL EFFECTS WITH VERTICAL GATE TRANSISTOR WITH

DIFFERENT **GATE MATERIALS**

FIG. 1a



ASPECT RATIO EQUATION

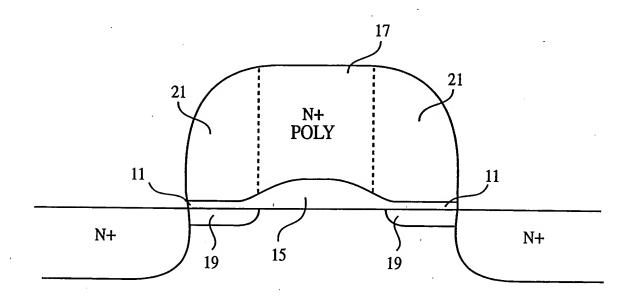
$$r = \frac{3L}{(W_{d} \cdot t_{OX} \cdot X_{j})}$$

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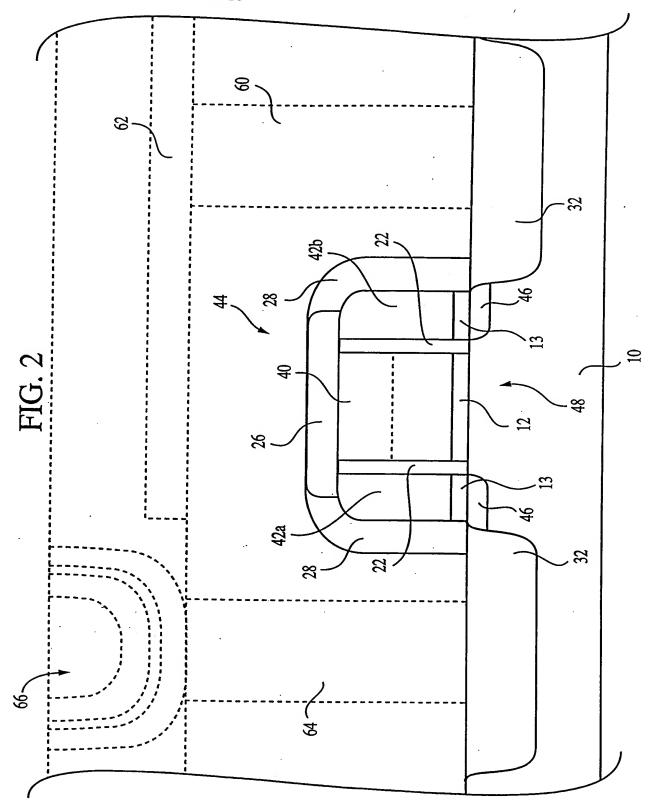
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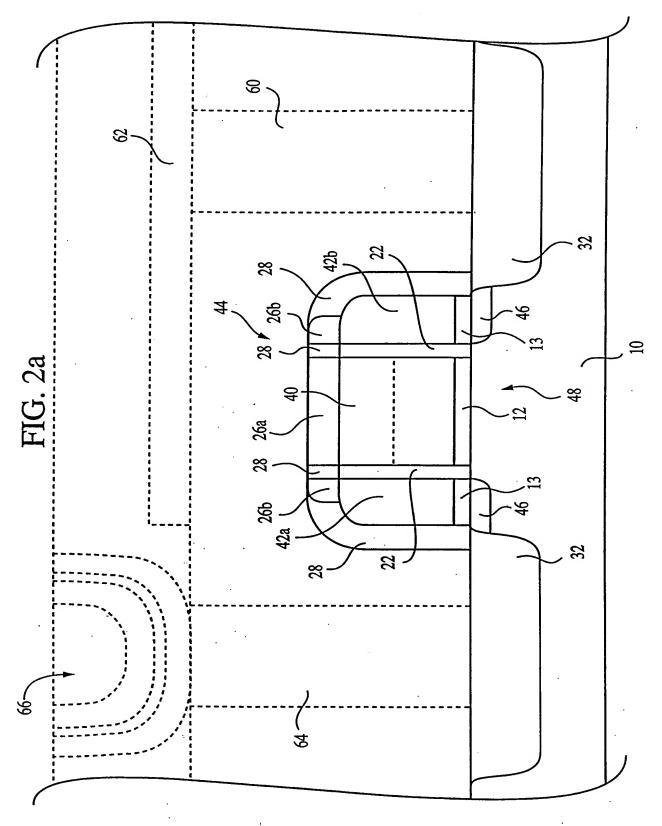
FIG. 1b



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FIG. 3a

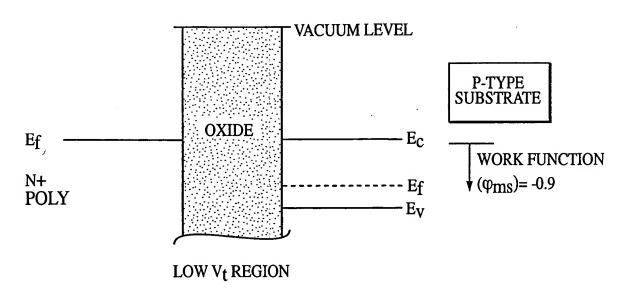


FIG. 3b

VACUUM LEVEL

P-TYPE SUBSTRATE

OXIDE E_c POLY E_f WORK FUNCTION $(\phi_{ms}) = +0.3$ HIGH V_t REGION

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FIG. 4

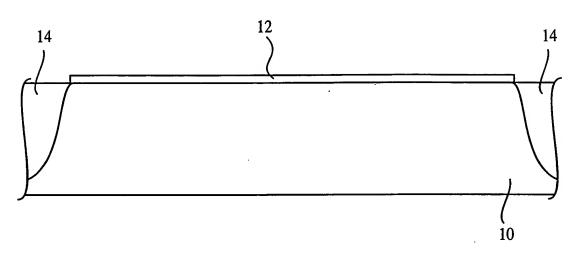
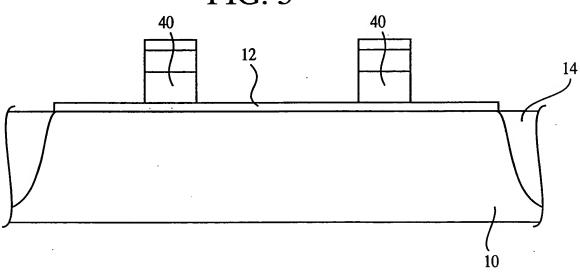


FIG. 5



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FIG. 6

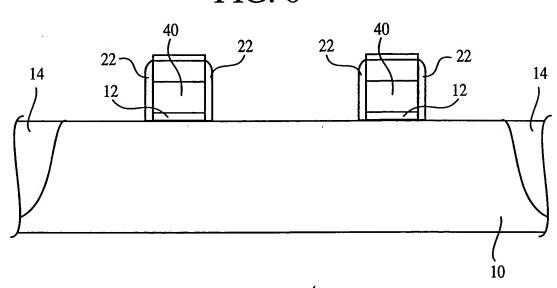
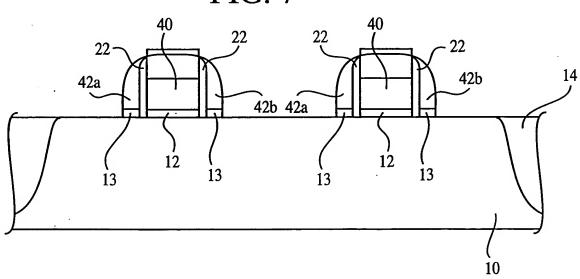


FIG. 7



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FIG. 8

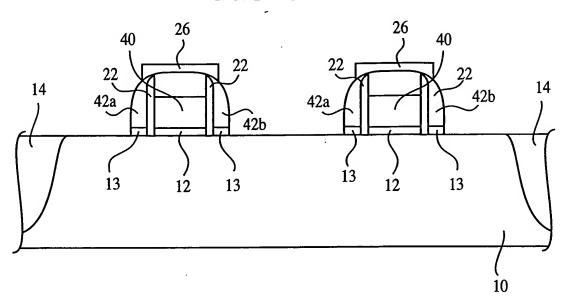
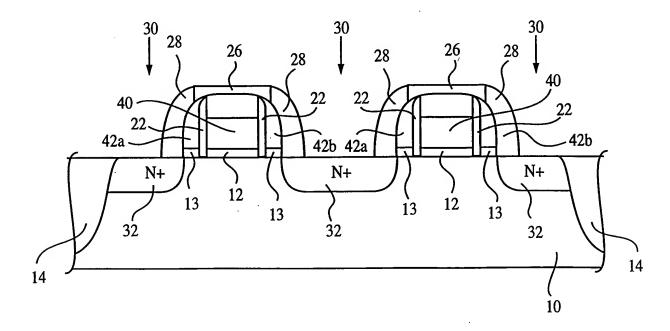


FIG. 9



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FIG. 10a

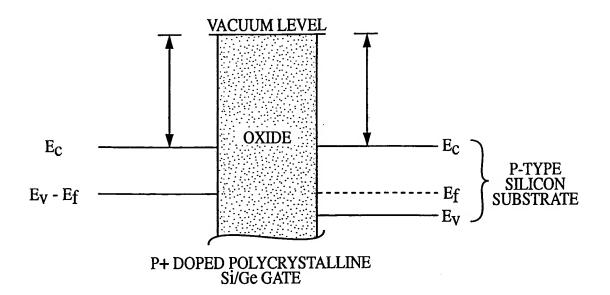
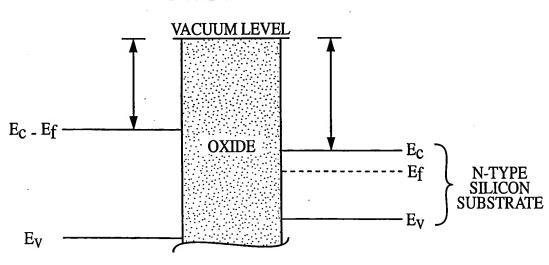


FIG. 10b



N+ DOPED SILICON CARBIDE COMPOUND (Si_{1-x}C_x) OR SILICON OXYCARBIDE

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FIG. 11

